Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A frequency monitor, comprising:

an edge detector which produces an output comprising a pulse for each rising/falling edge of an error signal, the error signal having a frequency responsive to a difference between frequencies of two input signals;

a conductive circuit having an effective resistance depending on a rate of the edge detector output pulses, wherein the conductive circuit comprises a switched capacitor circuit which charges and discharges at a rate that depends on the rate of the edge detector output pulses;

a capacitor which holds a charge responsive to the effective average resistance of the conductive circuit; and

an indicator circuit which produces an output responsive to the charge held by the capacitor.

2. Cancel claim 2.

3. (Original) The frequency monitor of Claim 1, wherein the indicator circuit comprises:

a comparator that produces the indicator circuit output, said output being at one of two levels based on the charge and a threshold, a first level indicating that the difference between

the two input signal frequencies is less than a predetermined amount, and the second level indicating that said difference is greater than a predetermined amount.

4. (Currently amended) A frequency monitor, comprising:

an edge detector which produces an output comprising a pulse for each rising/falling edge of an error signal, the error signal having a frequency responsive to a difference between frequencies of two input signals;

a conductive circuit having an effective resistance depending on a rate of the edge detector output pulses, wherein the conductive circuit comprises a switched capacitor circuit which charges and discharges at a rate that depends on the rate of the edge detector output pulses;

a capacitor which holds a charge responsive to the effective average resistance of the conductive circuit;

an indicator circuit which produces an output responsive to the charge held by the capacitor; and

a selector which, responsive to the indicator circuit output, selects from plural sources to control an oscillator.

5. (Original) The frequency of Claim 4, wherein the oscillator is a voltage-controlled oscillator.

6. (Original) The frequency monitor of Claim 4, wherein the plural sources are a data phase detector circuit and a frequency acquisition circuit.

7. (Original) The frequency monitor of Claim 6, wherein the oscillator produces a cloak signal at a sampling frequency, the clock signal being used by the detector circuit to receive data.

8. (Original) The frequency monitor of Claim 7, wherein the frequency acquisition circuit compares the clock signal with a reference clock to produce a frequency acquisition output indicative of a difference between the frequencies of the reference clock and the oscillator clock signal, said output being one of the sources to the selector.

9. (Original) The frequency monitor of Claim 7, wherein the data phase detector circuit compares the clock signal with a rate of incoming data to produce a data phase detector output indicative of a difference between the frequencies of the reference clock and the incoming data, said output being one of the sources to the selector.

10. (Original) The frequency monitor of Claim 9, wherein the data phase detector circuit output comprises the error signal.

11. (Currently amended) A frequency monitor, comprising:

a combiner circuit which combines two input signals to produce an error signal, the error signal having a frequency responsive to a difference between frequencies of the two input signals, wherein the combiner circuit comprises a mixer which mixes the two input signals to produce a mixed signal; and a low-pass filter which filters the mixed signal to produce the error signal;

an edge detector which produces an output comprising a pulse for each rising/falling edge of the error signal;

a conductive circuit having an effective resistance depending on a rate of the edge detector output pulses;

a capacitor which holds a charge responsive to the effective average resistance of the conductive circuit;

an indicator circuit which produces an output responsive to the charge held by the capacitor.

Cancel claims 12-16.

17. (Currently amended) A method for monitoring frequency, comprising:

producing an output comprising a pulse for each rising/falling edge of ~~the~~ error signal, the error signal having a frequency responsive to a difference between frequencies of two input signals;

charging a capacitor to a charge responsive to the frequency of the error signal ~~frequency~~; ~~and~~

indicating, responsive to the charge held by the capacitor, whether a difference between the two input signal frequencies is less than a predetermined amount~~.~~ ;and

using a switched capacitor circuit to charge the capacitor, the switched capacitor circuit having an effective resistance that depends on error signal frequency.

Cancel claim 18.

19. (Currently amended) A method for monitoring frequency, comprising:

producing an output comprising a pulse for each rising/falling edge of an error signal, the error signal having a frequency responsive to a difference between frequencies of two input signals;

charging a capacitor to a charge responsive to the error signal frequency;

indicating responsive to the charge held by the capacitor, whether a difference between the two input signal frequencies is less than a predetermined amount; ~~and~~

selecting, responsive to the step of indicating, from plural sources to control an oscillator; and combining the two input signals to produce the error signal.

20. (Original) The method of Claim 19, wherein the oscillator is a voltage-controlled oscillator.

21. (Original) The method of Claim 19, wherein the plural sources are a data phase detector circuit and a frequency acquisition circuit.

22. (Original) The method of Claim 21, wherein the oscillator produces a clock signal at a sampling frequency, the clock signal being used by the detector circuit to receive data.

23. (Original) The method of Claim 22, wherein the frequency acquisition circuit compares the clock signal with a reference clock to produce a frequency acquisition output

indicative of a difference between the frequencies of the reference clock and the oscillator clock signal, said output being one of the sources to the selector.

24. (Original) The method of Claim 22, wherein the data phase detector circuit compares the clock signal with a rate of incoming data to produce a data phase detector output indicative of a difference between the frequencies of the reference clock and the incoming data, said output being one of the sources to the selector.

25. (Original) The method of Claim 24, wherein the data phase detector circuit output comprises the error signal.

26. (Currently amended) A method for monitoring frequency, comprising:

combining two input signals to produce an error signal, the error signal having a frequency responsive to a difference between frequencies of two input signals, comprising mixing the two input signals to produce a mixed signal; and filtering, with a low-pass filter, the mixed signal to produce the error signal;

producing an output comprising a pulse for each rising/falling edge of the error signal;

charging a capacitor to a charge responsive to the error signal frequency; and

indicating, responsive to the charge held by the capacitor, whether a difference between the two input signal frequencies is less than a predetermined amount.

Cancel claims 27-36.

37. (Original) The frequency monitor of Claim 4, wherein the indicator circuit comprises:

a comparator that produces the indicator circuit output, said output being at one of two levels based on the charge and a threshold, a first level indicating that the difference between the two input signal frequencies is less than a predetermined amount, and the second level indicating that said difference is greater than a predetermined amount.

38. (Currently amended) ~~The~~ A frequency monitor ~~of Claim 34 wherein the combiner circuit comprises:~~, comprising:

an edge detector which produces an output comprising a pulse for each rising/falling edge of an error signal, the error signal having a frequency responsive to a difference between frequencies of two input signals;

a conductive circuit having an effective resistance depending on a rate of the edge detector output pulses;

a capacitor which holds a charge responsive to the effective average resistance of the conductive circuit;

an indicator circuit which produces an output responsive to the charge held by the capacitor;

a combiner circuit which combines the two input signals to produce the error signal; and

a selector which, responsive to the indicator circuit output, selects from plural sources to control an oscillator.

39. (Original) The frequency monitor of Claim 38, wherein the combiner circuit comprises:

a mixer which mixes the two input signals to produce a mixed signal; and

a low-pass filter which filters the mixed signal to produce the error signal.

40. (Original) The method of Claim 19, further comprising:

using a switched capacitor circuit to charge the capacitor, the switched capacitor circuit having an effective resistance that depends on error signal frequency.

Cancel claim 41.

42. (Original) The method of Claim ~~41~~ 19, wherein the step of combining comprises:

mixing the two input signals to produce a mixed signal; and

filtering, with a low-pass filter, the mixed signal to produce the error signal.

43. (Currently amended) ~~The~~ A frequency monitor ~~of Claim 11~~, comprising:

an edge detector which produces an output comprising a pulse for each rising/falling edge of an error signal, the error signal having a frequency responsive to a difference between frequencies of two input signals;

a conductive circuit having an effective resistance depending on a rate of the edge detector output pulses, wherein the conductive circuit comprises a switched capacitor circuit which charges and discharges at a rate that depends on the rate of the edge detector output pulses;

a capacitor which holds a charge responsive to the effective average resistance of the conductive circuit; and

an indicator circuit which produces an output responsive to the charge held by the capacitor.

44. (Original) The frequency monitor of Claim 11, wherein the indicator circuit comprises:

a comparator that produces the indicator circuit output, said output being at one of two levels based on the charge and a threshold, a first level indicating that the difference between the two input signal frequencies is less than a predetermined amount, and the second level indicating that said difference is greater than a predetermined amount.

45. (Currently Amended) ~~The~~ A method ~~of Claim 26~~ for monitoring frequency, ~~further~~ comprising:

combining two input signals to produce an error signal, the error signal having a frequency responsive to a difference between frequencies of two input signals;

producing an output comprising a pulse for each rising/falling edge of the error signal;

charging a capacitor to a charge responsive to the error signal frequency;

using a switched capacitor to charge the capacitor, the switched capacitor having an effective resistance that depends on error signal frequency; and

indicating, responsive to the charge held by the capacitor, whether a difference between the two input signal frequencies is less than a predetermined amount.